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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/694,574 | 10/24/2000 | Young Jin Oh | 8733.007.01 | 2428 |

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| EXAMINER | |
|---|---|
| QI, ZHI QIANG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2871 | |

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/694,574 | OH ET AL. | |
| | Examiner | Art Unit | |
| | Mike Qi | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *42-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/079/895* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 42-52, 54-55 and 56-66, 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,852,485 (Shimada et al) in view of US 6,040,886 (Ota et al).

Claims 42 and 56, Shimada disclose (col.11 line 1 – col. 12, line 63; Figs.1-3) that an in-plane switching liquid crystal device comprising:

- active-matrix substrate (128) and counter substrate (127), i.e., first and second substrates;
- a plurality of gate bus lines (13) and source bus lines (14) (acting as data bus lines) on the first substrate (128), the gate lines (13) being crossed with the data bus lines (14);
- a common line (125) parallel to the gate lines (13) on the first substrate (128);
- a gate insulation layer (115) on the fist substrate lower plate (120);
- the picture element electrode (12, 16) and the counter electrode (11) are formed of conductive material, e.g., ITO transparent conductive material, on the interlayer insulation layer (19) and the gate insulation layer (115), and even though the pixel electrode (12) and the common electrode (11) are not

directly on the gate insulating layer (115), but both of them are on the gate insulating layer (115), such that the transparent first metal layer (pixel electrode) and the transparent second metal layer (common electrode) are disposed on the gate insulating layer(115).

Ota discloses (col.6, line 33 – col.8, line 38; Fig.1) that the pixel electrode (3) and the common electrode (5) are formed on the gate insulation film (7). Because the pixel electrode and the common electrode are formed on the same layer and the same process as those signal electrodes (2,18), so that would simplify the manufacture process.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode and the common electrode formed on the gate insulator as claimed in claims 42 and 56 for achieving simplify manufacture process.

Claims 43-44 and 57-58, Shimada disclose (col. 11, line 15 – col.12, line21, Figs.1-3) that a TFT (122) is at each of the intersections of the gate lines (13) and the source lines (14), i.e., a plurality of thin film transistors at crossing points of the gate bus lines and the data bus lines, and the TFT (122) includes a gate electrode (15) on the first substrate lower plate (120), a semiconductor layer (114) on the gate electrode (15), source electrodes (111) and drain electrodes (112) on the semiconductor layer (114).

Claims 45-46 and 59-60, Shimada disclose (col.11, lines 31-53; Figs.1-3) that the drain electrode (112) is connected to the picture element electrode (12 as the transparent first metal layer) through a connecting electrode (16) and a contact hole

(17), the source electrode (111) is connected to the source line (14 as data line), and each counter electrode (as the second transparent metal layer) is connected to the common line through contact hole (col. 4, lines 23-26), i.e., the transparent second metal layer is connected to the common line.

Claims 47-48 and 61-62, Shimada disclose (col. 11, lines 32-53; Figs.1-3) that the connecting electrode (16) is connected to the picture element electrode (12), so that the electrode (16) also functions as pixel electrode, and the part of the electrode (16) overlapping the common line to form a storage capacitor. The part of the electrode (16) also overlapping the counter electrode (11) (Fig.3), so that forming another storage capacitor

Claims 49-50 and 63-64, Shimada disclose (col.12, lines 58-63; Figs.1-3) that the picture element electrode (12, 16) and the counter electrode (11) are formed of conductive material, e.g., ITO transparent conductive material, i.e., a transparent first metal layer (data electrode or pixel electrode) and a transparent second metal layer (counter electrode or common electrode).

Claims 51-52, 54-55 and 65-66,68-69, Shimada disclose (col.13, line 66 – col. 14, line 9; Figs 1-3) that a first alignment layer (116) on the first substrate (128) and the second alignment layer (117) on the second substrate (127), and the material for the alignment layer is polyimide.

3. Claims 53 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada and Ota as applied to claims 42-52, 54-55 and 56-66, 68-69 above, and further in view of US 5,929,958 (Ohta et al).

Claims 53 and 67, Ohta discloses (col.19, lines 26-39, col.20, lines 26-37; Fig.7) that an in-plane liquid crystal display device comprising a black matrix (BM) layer on the second substrate (SUB2), a color filter (FIL) on the black matrix layer (BM) and a liquid crystal layer (LC) between the first and second substrates (SUB1, SUB2), such that to improve the contrast and to prevent external light goes to the semiconductor layer (AS) of the TFT, so that protecting the TFT, and using color filter to display color signal.

Therefore, it would have been obvious to those skilled in the art at time the invention was made to arrange the black matrix, color filters as claimed in claims 53 and 67 for improving the contrast and display color signal.

***Response to Arguments***

4. Applicant's arguments filed on Aug.26, 2002 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) Shimada reference does not disclose the transparent first metal layer (pixel electrode) and the transparent second metal layer (counter electrode or common electrode) are formed on the gate insulator.

Examiner's responses to Applicant's **only** arguments are as follows:

1) Shimada discloses (col.11 line 1 – col. 12, line 63; Figs.1-3) that the pixel

electrodes and the common electrodes are formed on the interlayer insulation layer (19) and the gate insulation layer (115); even though the pixel electrode (12) and the common electrode (11) are not directly on the gate insulating layer (115), but both of them are on the gate insulating layer (115), such that the transparent first metal layer (pixel electrode) and the transparent second metal layer (common electrode) are disposed on the gate insulating layer(115). Ota discloses (col.6, line 33 – col.8, line 38; Fig.1) that the pixel electrode (3) and the common electrode (5) are formed on the gate insulation film (7). Because the pixel electrode and the common electrode are formed on the same layer and the same process as those signal electrodes (2,18), so that would simplify the manufacture process. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode and the common electrode formed on the gate insulator for achieving simplify manufacture process.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213. The examiner can normally be reached on 349.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Sikes can be reached on (703) 308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7721 for regular communications and (703) 308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
October 15, 2002

TOANTON
PRIMARY EXAMINER